

SN74LV07A Hex Buffers/Drivers With Open-Drain Outputs

1 Features

- 2-V to 5.5-V V_{CC} Operation
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Outputs are Disabled During Power Up and Power Down With Inputs Tied to V_{CC}
- Support Mixed-Mode Voltage Operation on All Ports
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model
 - 200-V Machine Model
 - 1000-V Charged-Device Model

2 Applications

- Servers
- Telecom Infrastructures
- TV Set-Top Boxes

3 Description

These hex buffers/drivers are designed for 2-V to 5.5-V V_{CC} operation.

The SN74LV07A device performs the Boolean function $Y = A$ in positive logic.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LV07A	TVSOP (14)	3.60 mm x 4.40 mm
	SOIC (14)	8.65 mm x 3.91 mm
	SOP (14)	10.30 mm x 5.30 mm
	SSOP (14)	6.20 mm x 5.30 mm
	TSSOP (14)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic

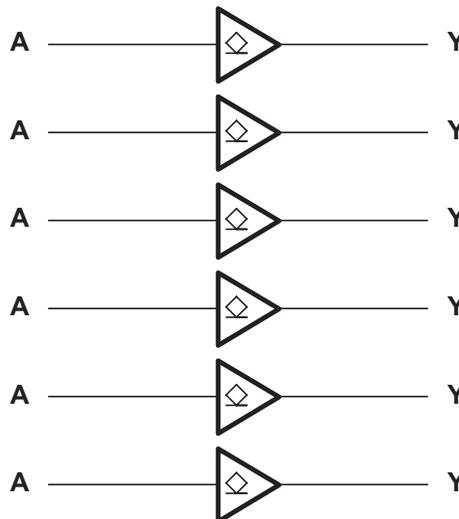


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5 Revision History

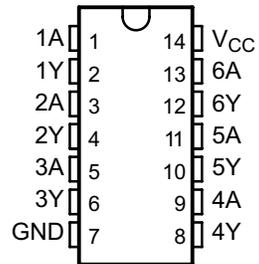
Changes from Revision J (October 2010) to Revision K

Page

• Updated document to new TI data sheet format	1
• Deleted Ordering Information table.	1
• Added Handling Ratings table.	4
• Changed MAX operating temperature to 125°C in Recommended Operating Conditions table.	4
• Added Thermal Information table.	5
• Added Typical Characteristics.	6
• Added Detailed Description section	7
• Added Application and Implementation section	8
• Added Power Supply Recommendations and Layout sections	9

6 Pin Configuration and Functions

SN74LV07A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	1	I	1A Input
1Y	2	O	1Y Output
2A	3	I	2A Input
2Y	4	O	2Y Output
3A	5	I	3A Input
3Y	6	O	3Y Output
4A	9	I	4A Input
4Y	8	O	4Y Output
5A	11	I	5A Input
5Y	10	O	5Y Output
6A	13	I	6A Input
6Y	12	O	6Y Output
GND	7	—	Ground Pin
V _{CC}	14	—	Power Pin

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	7	V
V _I	Input voltage range ⁽²⁾	-0.5	7	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	7	V
I _{IK}	Input clamp current	V _I < 0	-20	mA
I _{OK}	Output clamp current	V _O < 0	-50	mA
I _O	Continuous output current	V _O = 0 to V _{CC}	-35	mA
Continuous current through V _{CC} or GND			±50	mA

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 Handling Ratings

		MIN	MAX	UNIT	
T _{stg}	Storage temperature range	-65	150	°C	
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	0	1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2	5.5	V
V _{IH}	High level input voltage	V _{CC} = 2 V	1.5	V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7	
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7	
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	
V _{IL}	Low level input voltage	V _{CC} = 2 V	0.5	V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3	
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3	
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3	
V _I	Input voltage	0	5.5	V
V _O	Output voltage	0	5.5	V
I _{OL}	Low level output current	V _{CC} = 2 V	50	μA
		V _{CC} = 2.3 V to 2.7 V	2	
		V _{CC} = 3 V to 3.6 V	8	
		V _{CC} = 4.5 V to 5.5 V	16	
Δt/Δv	Input transition rise and fall rate	V _{CC} = 2.3 V to 2.7 V	200	ns/V
		V _{CC} = 3 V to 3.6 V	100	
		V _{CC} = 4.5 V to 5.5 V	20	
T _A	Operating free-air temperature	-40	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs (SCBA004)*.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LV07A					UNIT
		D	DB	DGV	NS	PW	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	100.6	112.5	135.2	95.4	128.7	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	51.8	65.0	57.9	52.9	57.2	
R _{θJB}	Junction-to-board thermal resistance	54.9	59.9	68.3	51.2	70.7	
ψ _{JT}	Junction-to-top characterization parameter	25.0	25.0	9.2	17.9	9.3	
ψ _{JB}	Junction-to-board characterization parameter	54.7	59.3	67.6	53.8	70.0	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN74LV07A			–40°C to 125°C SN74LV07A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V			0.1			0.1	V
	I _{OL} = 2 mA	2.3 V			0.4			0.4	
	I _{OL} = 8 mA	3 V			0.44			0.44	
	I _{OL} = 16 mA	4.5 V			0.55			0.55	
I _I	V _I = 5.5 V or GND	0 to 5.5 V			±1			±1	μA
I _{OH}	V _I = V _{IH} , V _{OH} = V _{CC}	5.5 V			±2.5			±2.5	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			20			20	μA
I _{off}	V _I or V _O = 0 to 5.5 V	0			5			5	μA
C _i	V _I = V _{CC} or GND	3.3 V		1.6			1.6		pF

7.6 Switching Characteristics, V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN74LV07A		–40°C to 125°C SN74LV07A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	C _L = 15 pF		6.6 ⁽¹⁾	10.4 ⁽¹⁾	1	13	1	14	ns
t _{PHL}	A	Y			7.5 ⁽¹⁾	10.4 ⁽¹⁾	1	13	1	14	
t _{PLH}	A	Y	C _L = 50 pF		11.1	15.2	1	18	1	19	ns
t _{PHL}	A	Y			9.6	15.2	1	18	1	19	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

7.7 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN74LV07A		–40°C to 125°C SN74LV07A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	C _L = 15 pF		5 ⁽¹⁾	7.1 ⁽¹⁾	1	8.5	1	9.5	ns
t _{PHL}	A	Y			5 ⁽¹⁾	7.1 ⁽¹⁾	1	8.5	1	9.5	
t _{PLH}	A	Y	C _L = 50 pF		8.2	10.6	1	12	1	13	ns
t _{PHL}	A	Y			6.6	10.6	1	12	1	13	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

7.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

 operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN74LV07A		$-40^\circ\text{C to } 125^\circ\text{C}$ SN74LV07A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	$C_L = 15\text{ pF}$		3.8	5.5 ⁽¹⁾	1	6.5	1	7.2	ns
t_{PHL}	A	Y			3.4 ⁽¹⁾	5.5 ⁽¹⁾	1	6.5	1	7.2	
t_{PLH}	A	Y	$C_L = 50\text{ pF}$		5.7	7.5	1	8.5	1	9.2	ns
t_{PHL}	A	Y			4.5	7.5	1	8.5	1	9.2	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

7.9 Noise Characteristics⁽¹⁾

 $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.4	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.1	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3.2		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

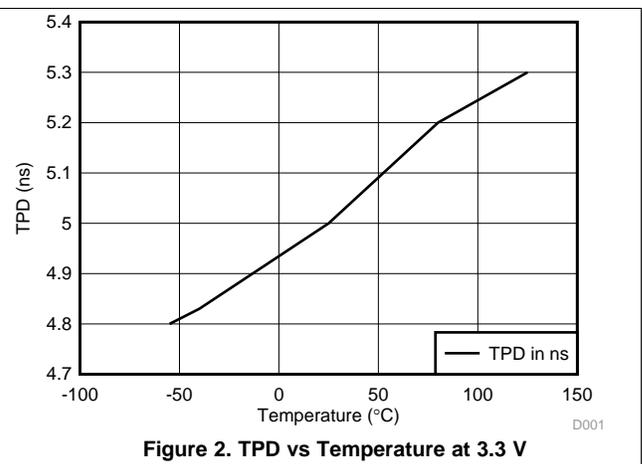
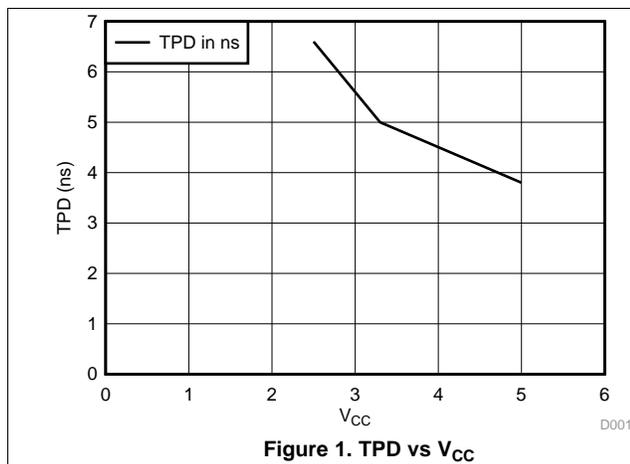
(1) Characteristics are for surface-mount packages only.

7.10 Operating Characteristics

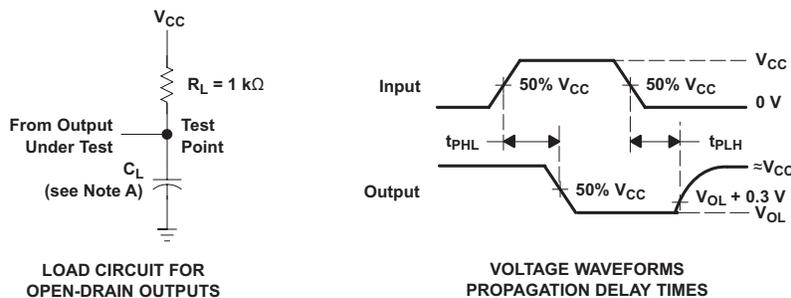
 $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$,	$f = 10\text{ MHz}$	3.3 V	2.9	pF
				5 V	5.3	

7.11 Typical Characteristics



8 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \ \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$.
- C. The outputs are measured one at a time, with one input transition per measurement.

Figure 3. Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

The outputs of the SN74LV07A device are open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 16 mA at 5-V V_{CC} . Inputs can be driven from 2.5-V, 3.3-V, or 5-V (CMOS) devices. This feature allows the use of the SN74LV07A device as a translator in a mixed-system environment. This device is fully specified for partial power-down applications using I_{off} . The I_{off} circuitry disables the outputs, thus preventing a damaging current backflow through the device when it is powered down.

9.2 Functional Block Diagram

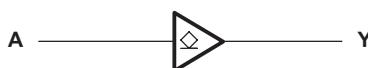


Figure 4. Logic Diagram, Each Buffer/Driver (Positive Logic)

9.3 Feature Description

- Wide operating voltage range
 - Operates from 2 V to 5.5 V
- Allows up or down voltage translation
 - Inputs and outputs accept voltages to 5.5 V
- I_{off} feature
 - Allows voltages on the inputs and outputs when V_{CC} is 0 V

9.4 Device Functional Modes

Table 1. Function Table
(Each Buffer/Driver)

INPUT A	OUTPUT Y
H	H
L	L

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN74LV07A device is a low drive, open-drain CMOS device that can be used for a multitude of buffer type functions. The inputs are 5.5-V tolerant. The outputs are open drain and 5.5-V tolerant; thus, allowing the device to translate up to 5.5 V or down to any other voltage between GND and 5.5 V.

10.2 Typical Application

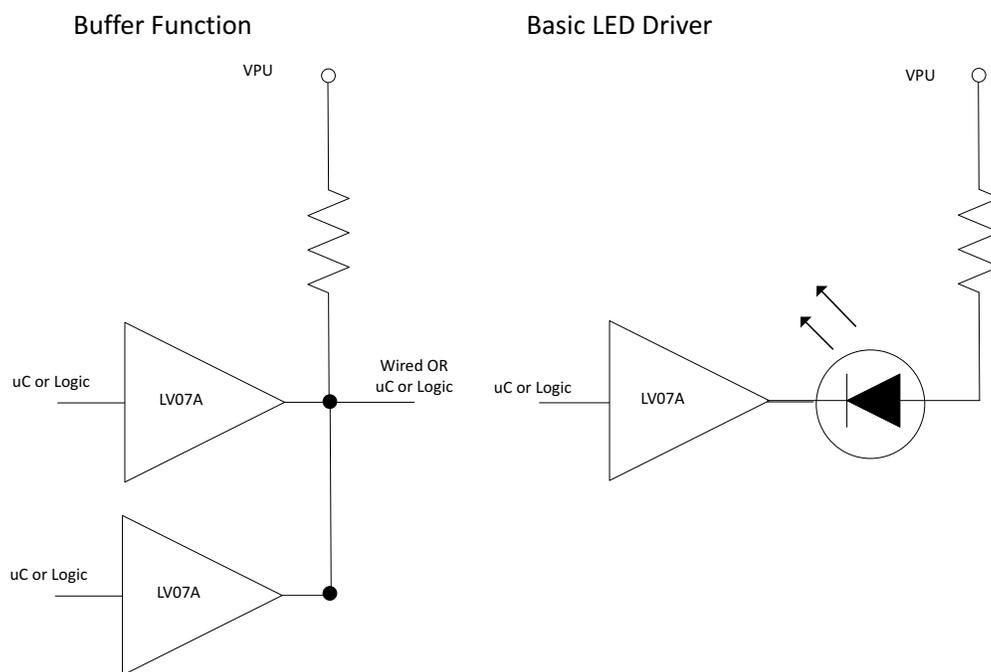


Figure 5. Typical Application Schematic

10.2.1 Design Requirements

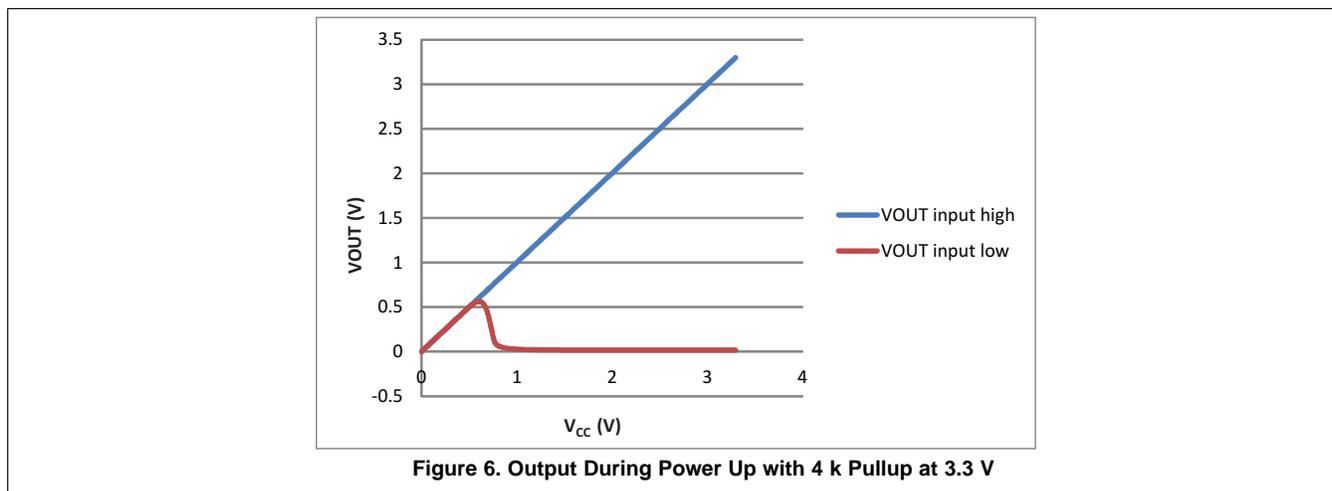
This device uses CMOS technology and is open drain, so it has low output drive only. Care should be taken to avoid bus contention, because it can drive currents that would exceed maximum limits. Parallel output drive can create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
 - For rise time and fall time specifications, see $\Delta t/\Delta V$ in the [Recommended Operating Conditions](#) table.
 - For specified high and low levels, see V_{IH} and V_{IL} in the [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .
2. Recommended Output Conditions:
 - Load currents should not exceed 35 mA per output and 50 mA total for the part.

Typical Application (continued)

10.2.3 Application Curves



11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#). Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended. If there are multiple V_{CC} terminals then 0.01 μF or 0.022 μF is recommended for each power terminal. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 7](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver.

12.2 Layout Example

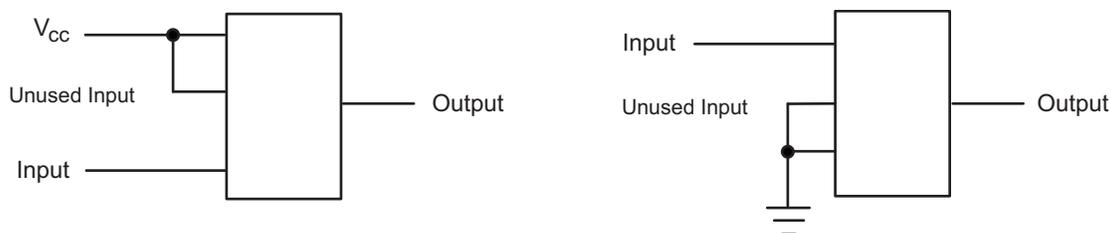


Figure 7. Layout Diagram

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV07A	Click here				

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV07AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV07A	Samples
SN74LV07ADBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV07A	Samples
SN74LV07ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV07A	Samples
SN74LV07ADGVR	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV07A	Samples
SN74LV07ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV07A	Samples
SN74LV07ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV07A	Samples
SN74LV07ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV07A	Samples
SN74LV07ANSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV07A	Samples
SN74LV07APW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV07A	Samples
SN74LV07APWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV07A	Samples
SN74LV07APWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV07A	Samples
SN74LV07APWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 125	LV07A	Samples
SN74LV07APWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV07A	Samples
SN74LV07APWRG3	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LV07A	Samples
SN74LV07APWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV07A	Samples
SN74LV07APWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV07A	Samples
SN74LV07APWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV07A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

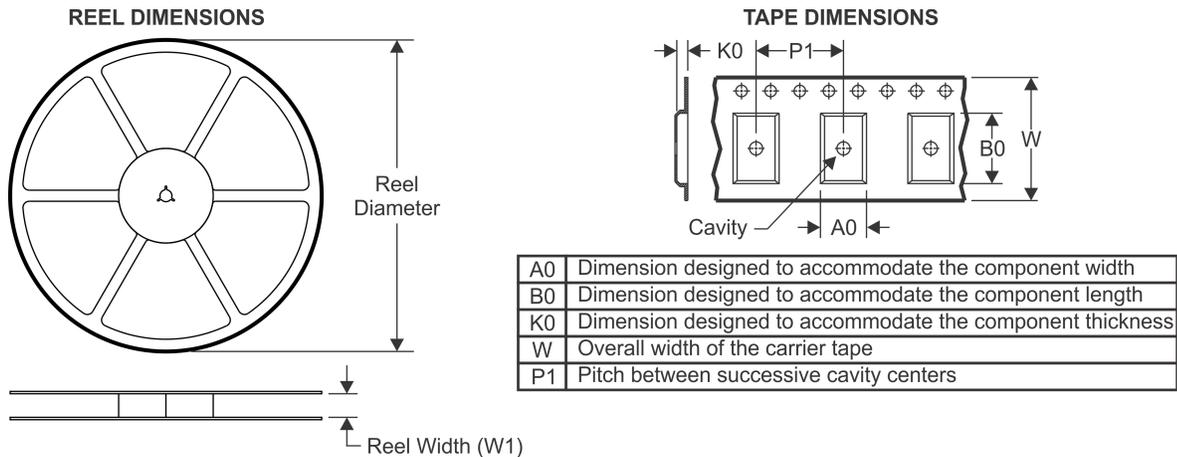
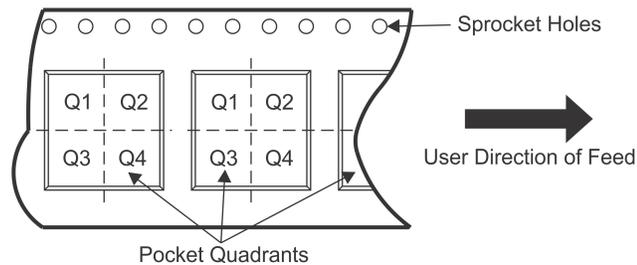
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

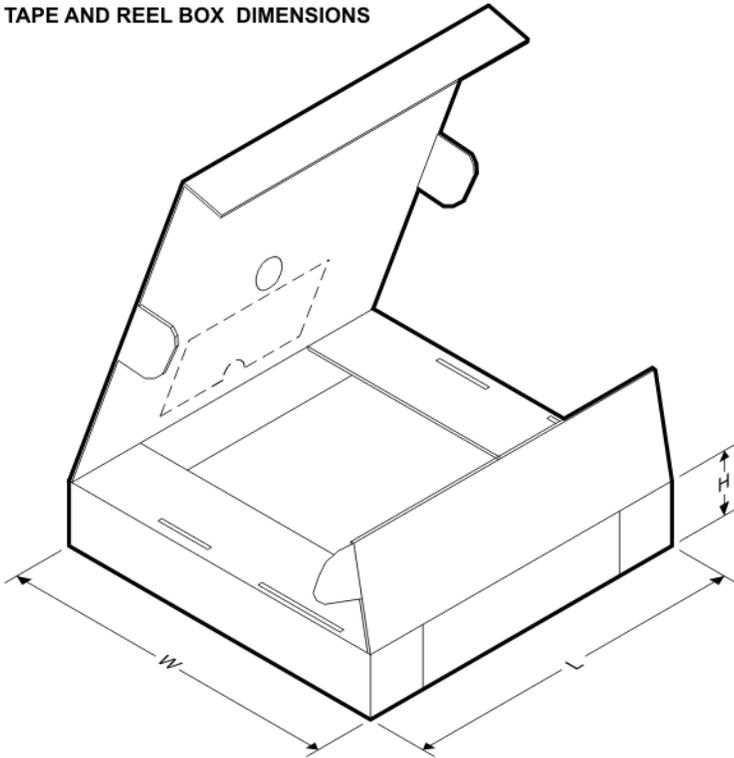
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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV07ADBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LV07ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV07ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV07APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV07APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV07APWRG3	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV07APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV07APWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


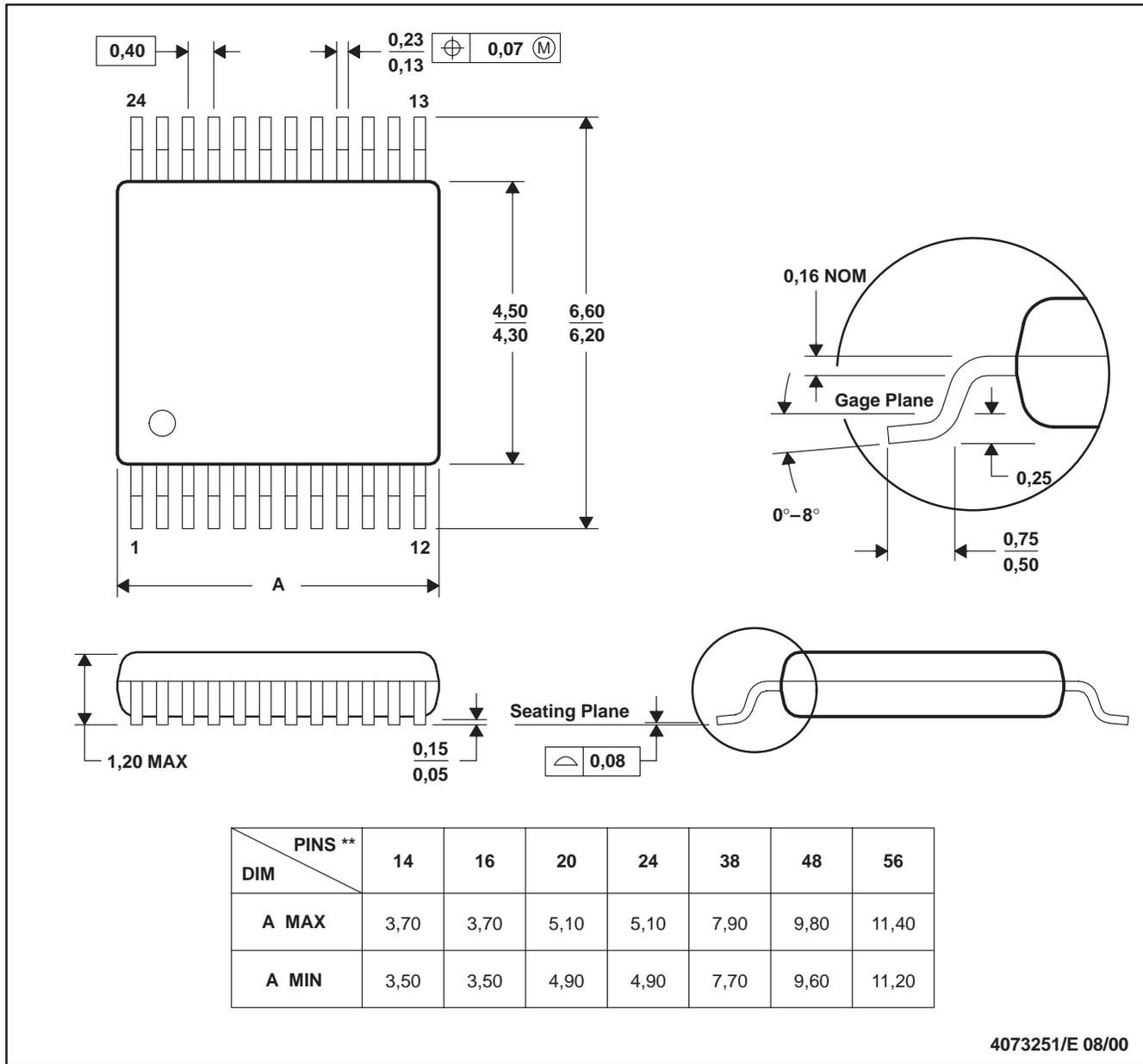
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV07ADBR	SSOP	DB	14	2000	367.0	367.0	38.0
SN74LV07ADGVR	TVSOP	DGV	14	2000	367.0	367.0	35.0
SN74LV07ADR	SOIC	D	14	2500	367.0	367.0	38.0
SN74LV07APWR	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74LV07APWR	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74LV07APWRG3	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74LV07APWRG4	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74LV07APWT	TSSOP	PW	14	250	367.0	367.0	35.0

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

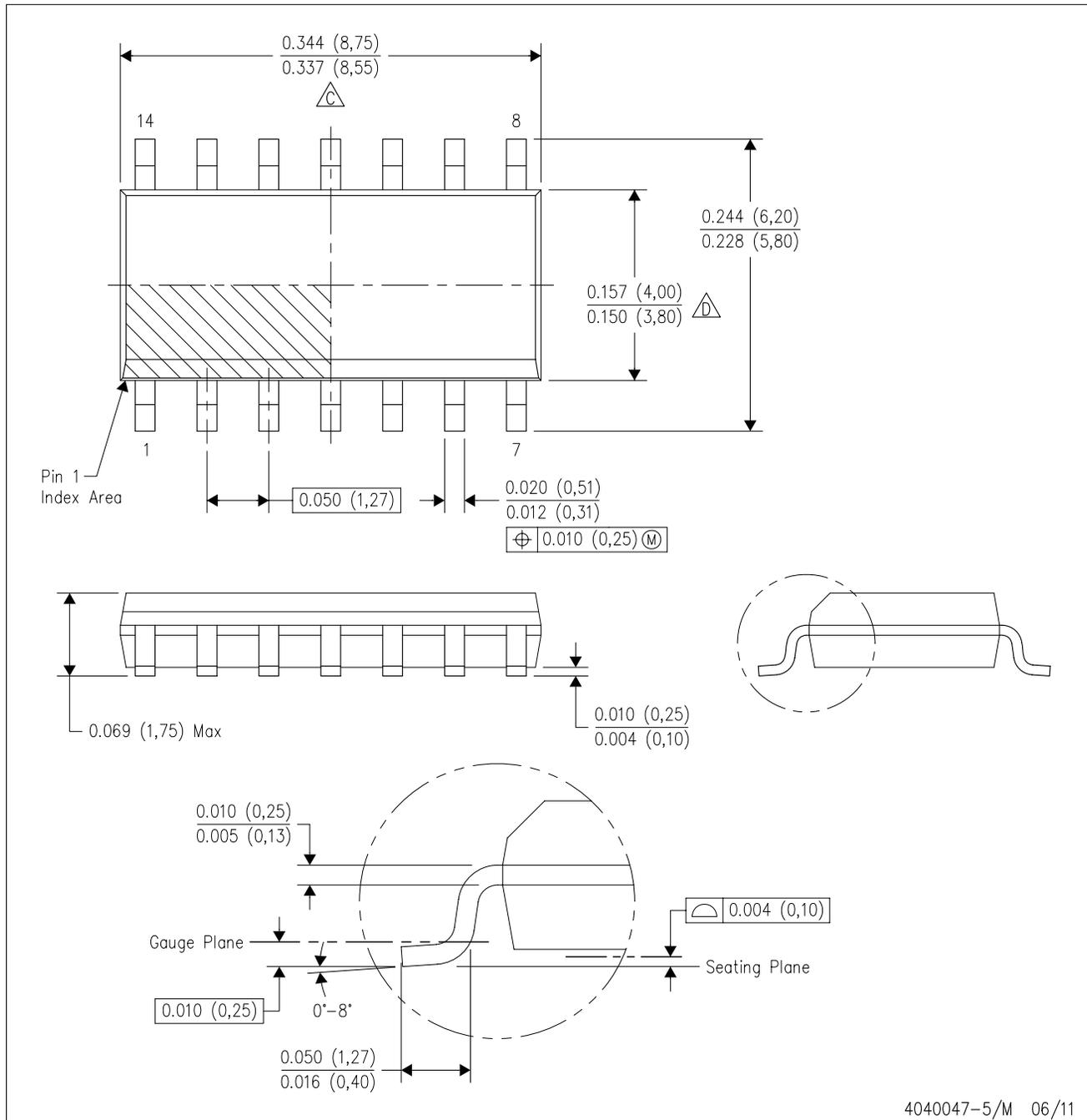


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- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

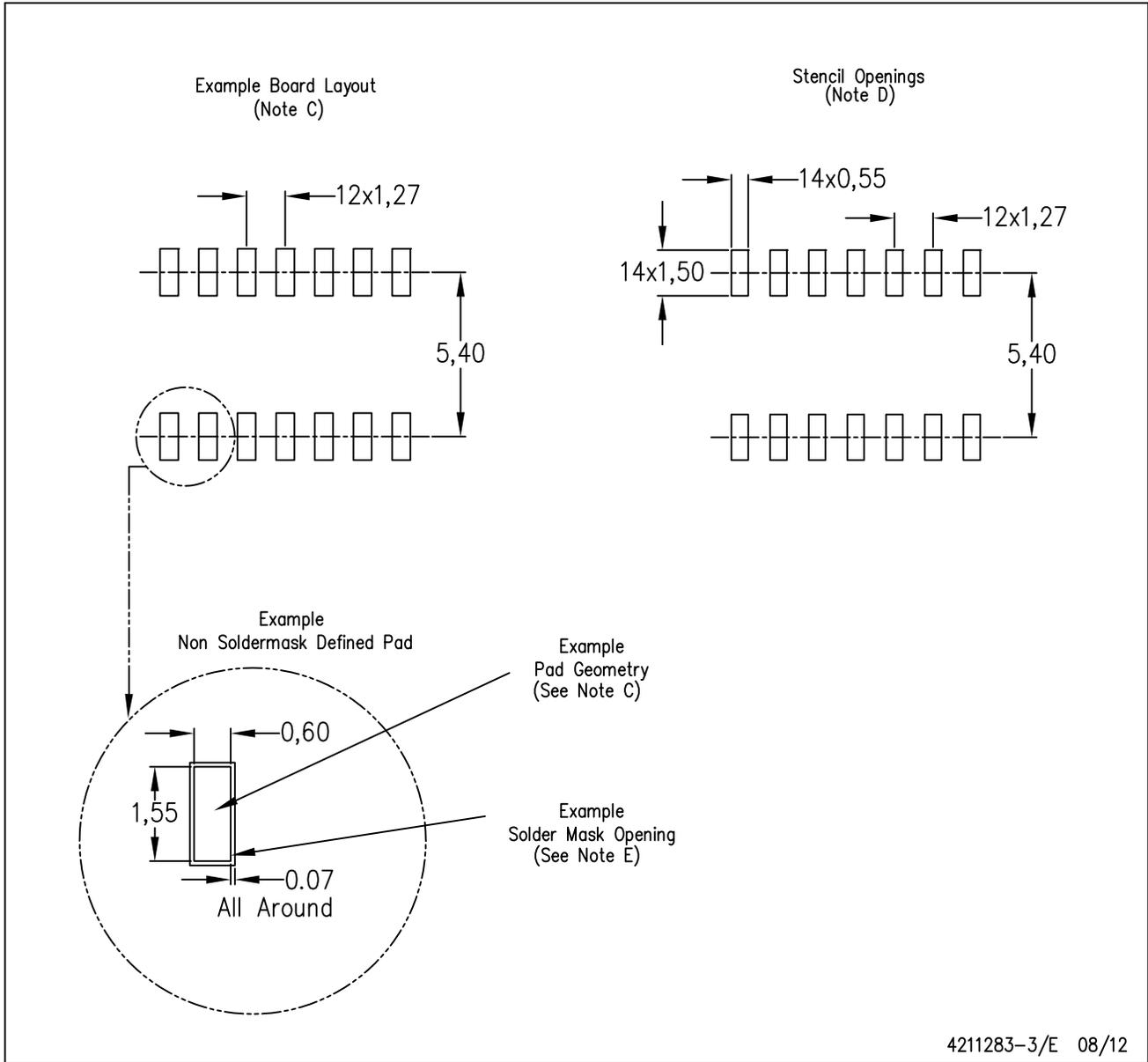
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

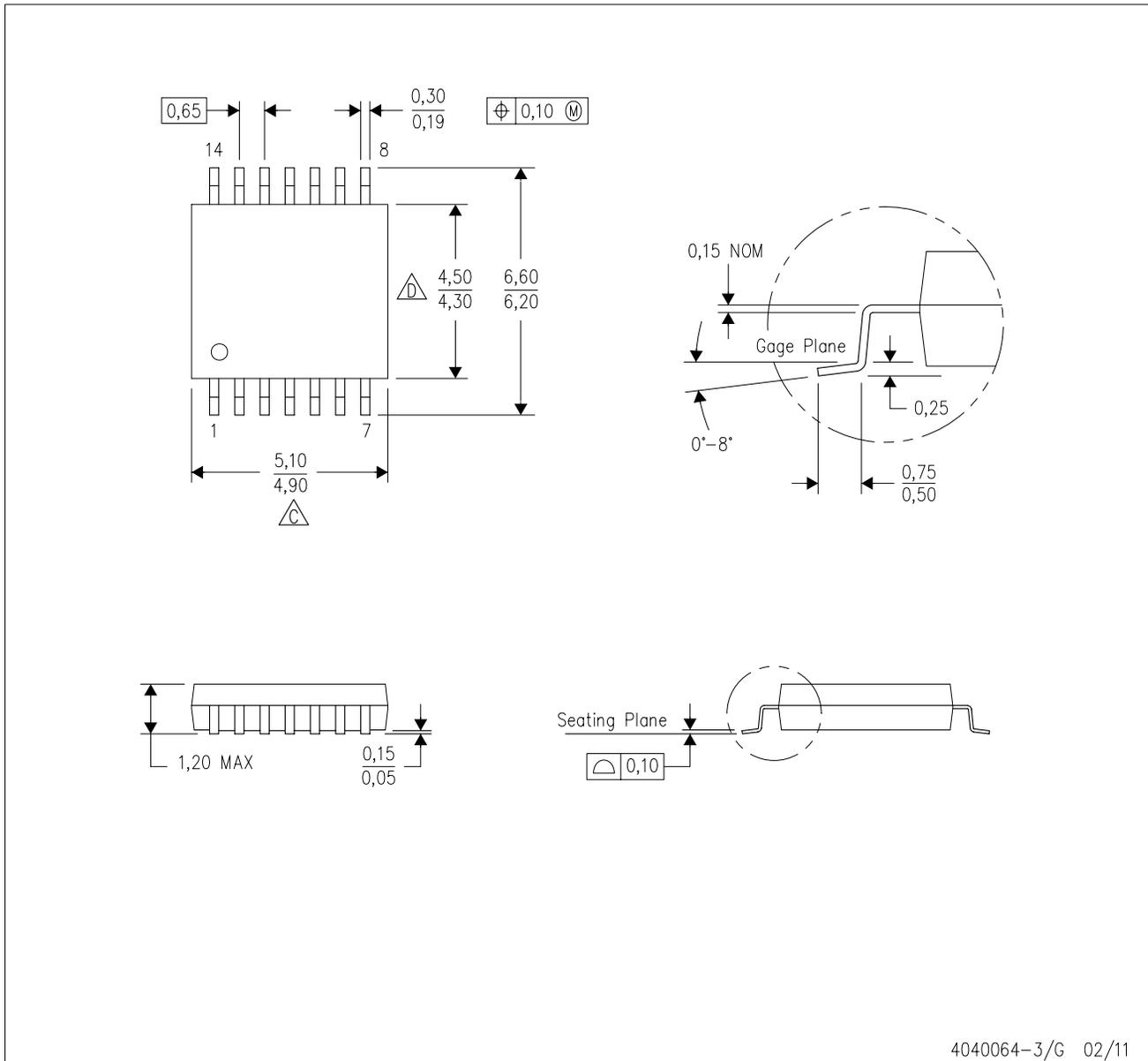
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

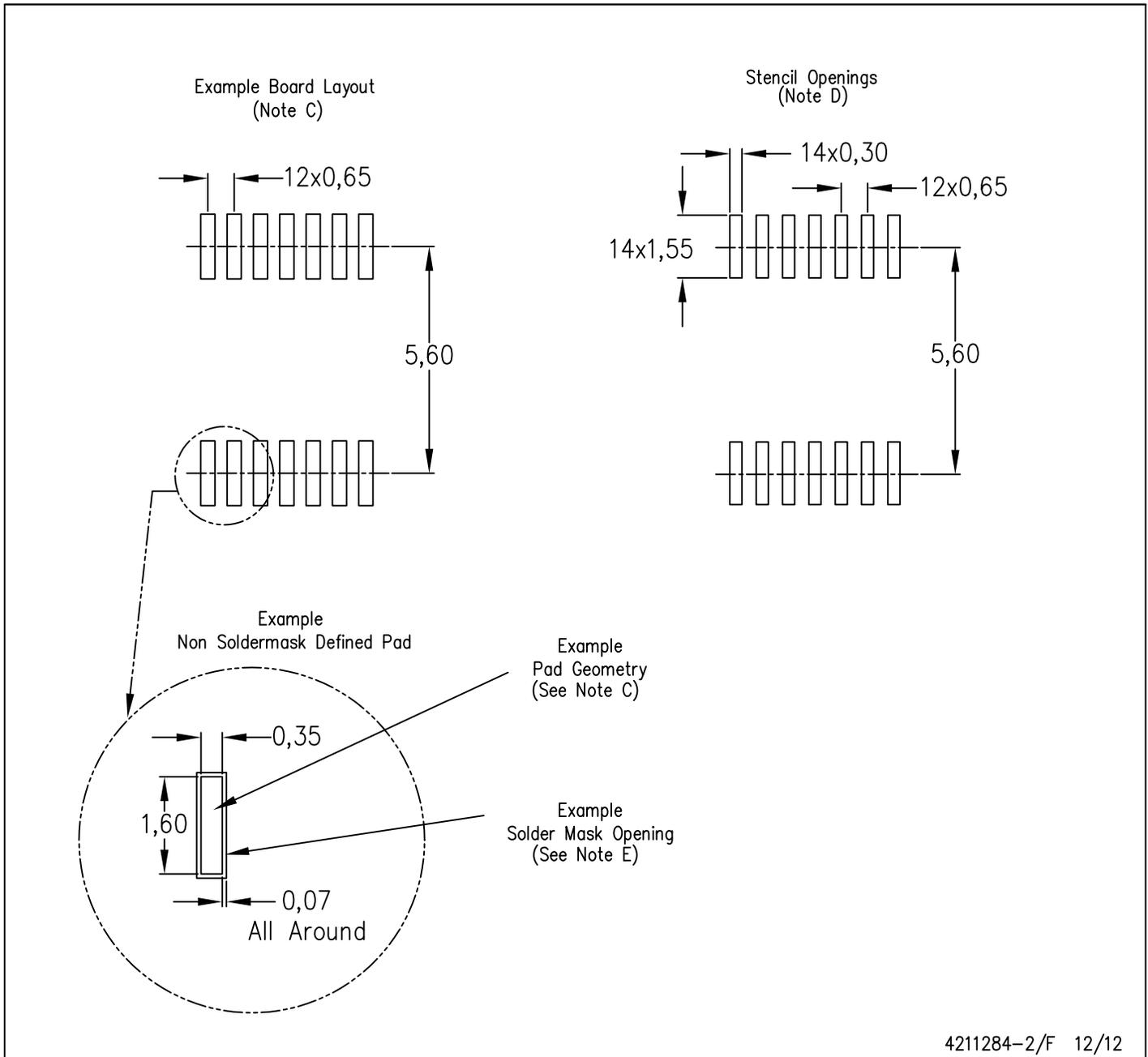
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



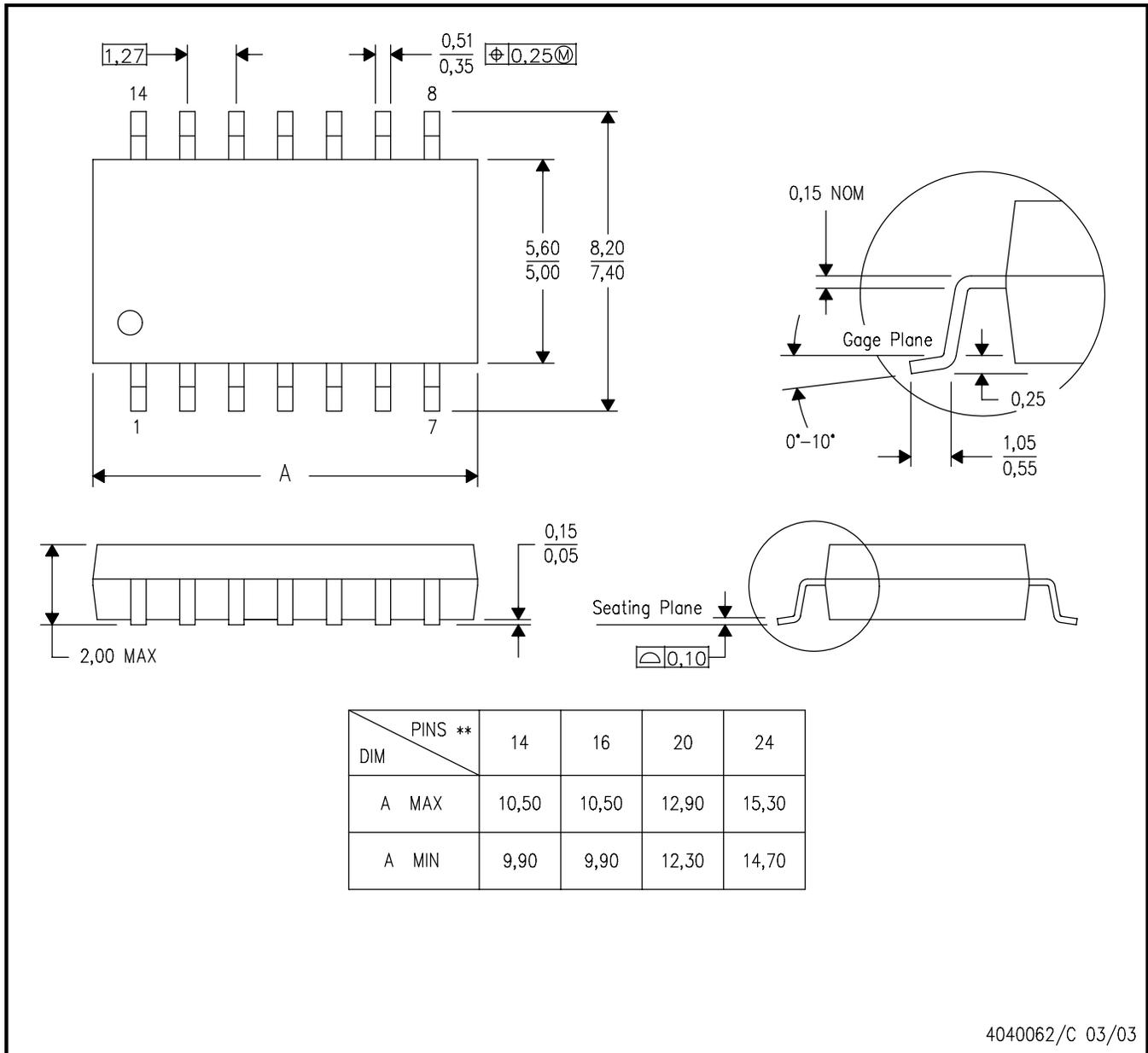
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

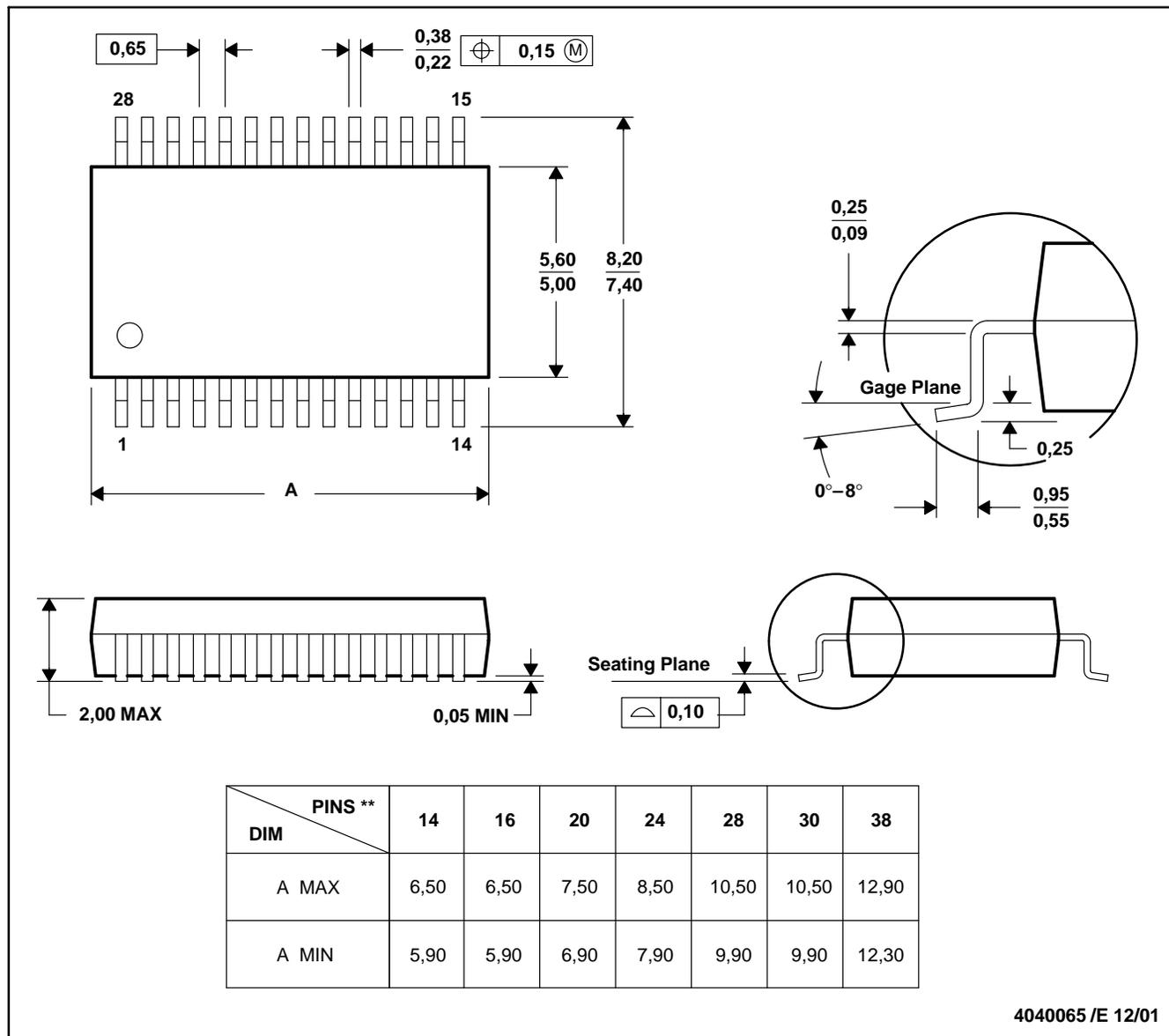


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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